THAT WHICH IS CLAIMED IS:

1. A microprocessor comprising an address bus, a data bus, a plurality of read accessible and write accessible registers and an address decoder to select said registers as a function of the address present in said address bus, wherein the microprocessor furthermore comprises a plurality of protection circuits each associated with a register of the microprocessor to secure the access to said register, said protection circuits automatically blocking the selection of said registers after each resetting of the microprocessor, and wherein the releasing of a protection circuit associated with a microprocessor register is done by the successive sending, on the data bus, of N passwords proper to said register during N first operations for the selection of said register with $N \geq 1$, the selection of said register being effective only for the subsequent operations for the selection of said register up to the next resetting of the microprocessor.

2. A microprocessor according to claim 1, wherein said protection circuit, after each resetting of the microprocessor, is arranged to block the selection of a register during operations of read access and write access to said register.

3. A microprocessor according to claim 1 wherein said protection circuit, after each resetting of the microprocessor, is arranged to block the selection of a register only during operations of write access to said register.

4. A microprocessor according to one of the claims 1 to 3, wherein each protection circuit is connected between an output of the address decoder

given the task of selecting the register associated with said protection circuit and an input for the selection of said associated register.

5. A microprocessor according to one of the claims 1 to 4, wherein each protection circuit, during the N first operations for the selection of the associated register, is arranged to compare the N data elements present on the data bus with the N passwords proper to said associated register and gets released for the subsequent operations of selection of said register up to the next resetting of the microprocessor if the N data elements correspond to the N passwords.

6. A microprocessor according to claim 4, wherein one password is provided for each register, and each protection circuit comprises:

- a comparator circuit for the comparison, during the first operation of selection of the associated register, of the data element present on the data bus with the password proper to said register and for the delivery of an output signal representing the result of the comparison,
- first means for the holding, in the protection circuit, of said output signal up to the following resetting of the microprocessor,
- second means to permit the selection of the register for the subsequent selection operations of said register if said output signal indicates that the data present in the data bus of the microprocessor during the first operation of selection of the register corresponds to the password associated with said register.

7. A microprocessor according to claim 6, wherein the first means comprise first and second D type flip-flop circuits, each having a clock input, a

signal input, a resetting input to which a signal for resetting the microprocessor is applied, and a signal output,

the first flip-flop circuit having its clock input connected to the output of the address decoder responsible for selecting the register associated with said protection circuit and its signal input that receives a signal corresponding to a logic « 1 »

and the second flip-flop circuit having its clock input connected to the signal output of the first flip-flop circuit, its signal input which receives the output signal of the comparator circuit and its output signal which thus delivers the output signal of the comparator circuit up to the next resetting of the microprocessor.

8. A microprocessor according to claim 7, wherein the second means comprises an AND type two-input logic gate having its first input is connected to the output of the address decoder which has the task of selecting the register associated with said protection circuit, its second input is connected through a delay circuit to the output signal of the second flip-flop circuit of the first means, and its output connected to the selection input of the associated register.

9. A microprocessor according to claim 8, wherein said delay circuit is a shift register synchronized with the operations for the selection of said register.